Form PTO 1449	Atty. Docket Number	Serial Number
U.S. Department of Commerce Patent and Trademark Office	HITA.0501	To be assigned
	Applicant SAITO et al	
Information Disclosure Statement by Applicant	Filing Date Concurrently herewith	Group

U.S. Patent Documents

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date

Foreign Patent Documents

Examiner Initial		Document Number	Filing Date	Country	Class	Sub-class	Translation	
							Yes	No
PC		2002-313951	4/11/2001	Japan			Abstract	X

Other Documents (Including Author, Title, Date Pertinent Pages, Etc.)

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PC		Patrick P. Gelsinger, "Microprocessors for the New Millennium: Challenges, Opportunities, and New Frontiers", 2001 IEEE International Solid-State Circuits Conference, 10 pages
PC		D.A. Buchanan et al. "80 nm Poly-silicon Gated n-FETs with Ultra-Thin Al_2O_3 Gate Dielectric for ULSI Applications", IEEE (2000), 4 pages
PC		K. Torii et al., "Fixed Charge-Induced Mobility Degradation and its Recovery in MISFET's with Al_2O_3 Gate Dielectric", IWGI 2001, Tokyo, pp. 230-232
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PC		Kunihiro Suzuki et al., "Scaling Theory for Double-Gate SOI MOSFET's", IEEE Transactions on Electron Devices, Vol. 40, No. 12, December 1993, pp. 2326-2329
PC		International Technology Roadmap for Semiconductors, 2001 Edition, "Front End Processes", pp. 1-44

Examiner	Date Considered
PHAT X. CAO	8/12/05

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